REMARKS

I. Introduction

In response to the Office Action dated August 16, 2004, Applicants have amended claims 12 and 13 so as to further clarify the claimed subject matter. Support for this amendment can be found, for example, at page 10, line 22 to page 13, line 15 and page 14, line 8 to page 15, line 1. No new matter has been added.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. The Rejection Of The Claims Under 35 U.S.C. § 102

Claims 12 and 13 are rejected under 35 U.S.C. § 102 as being anticipated by USP No. 6,092,208 to Reneris. Applicants respectfully traverse this rejection for at least the following reasons.

Claim 12 recites in-part a method for designing, at specification, architectural or RT level, a semiconductor integrated circuit device including a plurality of blocks, each block including a plurality of cells, the method comprising the step of c) generating priority-order-controlling information for the respective blocks based on the priority-order information as to the respective functional units within each said block and the interconnection information about the top-level hierarchy.

In accordance with one embodiment of the present invention, the "top-level hierarchy" represents the overall system, ranging from the lowest to the highest level layers (i.e., specification level, architectural level and RT level layers). Specifically, as shown in step ST35, information about the order of priority applicable to respective functional units is defined. For example, the

power management function may be given the highest priority, the internal error management function may be given the second highest priority and the external input acceptance function may be given the third highest priority. In this manner, the respective functions are assigned an appropriate order of priority. Next, in step ST36, an inter-block priority order control module is generated based on the information about the priority order, as defined in step ST35, and the interconnection information about the top-level hierarchy as defined in step ST37. In step ST38, information about the priority order with each block is defined. Then, in step ST39, an intra-block priority order control module is generated based on the definition (see, e.g., page 15, line 20 to page 16, line 11). The foregoing method provides an optimized semiconductor device to meet various requirements imposed by the electronic industries, such as downsizing and reduced power dissipation, by designing the overall device at the specification, architectural or RT level, while using the design data for the respective blocks (see, e.g., page 4, lines 4-10 of the specification).

Turning to the cited prior art, it is asserted in the Office Action that Reneris discloses, at col. 2, lines 21-33, generating priority-order controlling information for the respective blocks based on the priority order information as to the respective functional units within each said block and the interconnection information about the top-level hierarchy.

However, in contrast to the conclusion set forth in the pending rejection, at the cited portion, Reneris discloses providing a system and method for managing power consumption in a computer system (i.e., power management of operating system such as Windows NT). Specifically, Reneris discloses that a computer program contained in a computer readable medium is executed for identifying power dependencies within a computer system using a set of data structures, such that the program instructions can determine which of the power resources must be on or off by reading the power management data structure. As such, nowhere does Reneris disclose or suggest any

priority order controlling information or top level hierarchy in the manner alleged by the Examiner. Indeed, the Examiner has neither identified which element of Reneris corresponds to the claimed priority order controlling information or top level hierarchy.

Thus, at a minimum, Reneris fails to disclose or suggest a method for designing, at specification, architectural or RT level, a semiconductor integrated circuit device including a plurality of blocks, each block including a plurality of cells, the method comprising the step of d) generating priority-order-controlling information for the respective blocks based on the priority-order information as to the respective functional units within each said block and the interconnection information about the top-level hierarchy, as recited by claim 12.

As anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, *Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983)*, and at a minimum, Reneris fails to disclose the foregoing claim elements, it is clear that Reneris does not anticipate claim 12 or any of the claims dependent thereon.

III. All Dependent Claims Are Allowable Because The Independent Claims From Which They Depend Are Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co., 819 F.2d at 1100, 1108 (Fed. Cir. 1987)*. Accordingly, as claim 12 is patentable for the reasons set forth above, it is respectfully submitted that claim 13 dependent thereon is also in condition for allowance.

For all of the foregoing reasons, it is submitted that claim 13 is patentable over the cited prior art. Accordingly, it is respectfully submitted that the rejections of claims 12 and 13 under 35 U.S.C. § 102 have been overcome.

IV. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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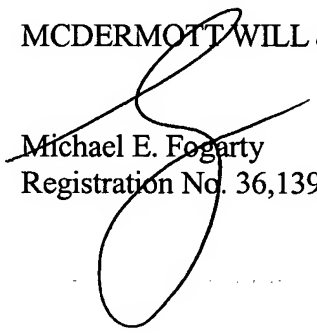

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